Two Stop-and-Go Gate Driving to Reduce Switching Loss and Switching Noise in Automotive IGBT Modules

Toshiaki Inuma[1], Katsuhiro Hata[1], Toru Sai[2], Wataru Saito[3], and Makoto Takamiya[1]
[1] The University of Tokyo, Tokyo, Japan
[2] Tokyo Polytechnic University, Kanagawa, Japan
[3] Kyushu University, Fukuoka, Japan

***Abstract*— A new active gate driving method of "two stop-and-go gate driving (2S&G)" is proposed to reduce both the switching loss (E_{LOSS}) and the collector current overshoot ($I_{OVERSHOOT}$) in the turn-on of automotive IGBT modules. 2S&G includes two gate current zeros during turn-on and has only two parameters for a digital gate driver, which means low test cost for parameter optimization. Five different gate driving methods, including the conventional single-step gate driving (CSG), the conventional one stop-and-go gate driving, and digital gate drivings with 100 ns × 4 slots and 20 ns × 20 slots, are compared in the double pulse test using a 6-bit digital gate driver IC at 300 V and 150 A, and the proposed 2S&G showed the best performance. Compared with CSG, the proposed 2S&G reduces E_{LOSS} by 42 % under $I_{OVERSHOOT}$-aligned condition and reduces $I_{OVERSHOOT}$ by 18 % under E_{LOSS}-aligned condition.**

Keywords*— *active gate driving, switching loss, switching noise, IGBT

I. Introduction

Digital gate drivers (DGDs), which digitally change the gate current (I_G) multiple times in fine time slots during the switching period of power devices, are attracting attention as a technology that can solve the trade-off problem between loss and noise during power device switching [2-8]. DGDs have the advantage that the I_G waveform can be flexibly changed by software, while they have the disadvantage that the driving parameters of DGDs (defined as gate vectors in this paper) have too many degrees of freedom, making it difficult to determine the optimal gate vector. For example, in [9], the optimal gate vector is searched by 15-min measurements using the particle swarm optimization among $(2^6)^{60}$ ($> 10^{180}$) possible combinations of a 60-slot 6-bit DGD, while the high test cost for the optimization is a challenge for practical applications. To reduce the test cost, a one stop-and-go gate driving (1S&G), which reduces the gate vector to one parameter, has been proposed and reported to show almost the same switching loss and noise reduction performance as a 4-slot digital gate driving in a small capacity IGBT (600 V, 100 A rating) [1]. This paper shows that the conventional 1S&G does not work effectively in the turn-on of a large-capacity automotive IGBT (1200 V, > 200 A rating), and proposes a new active gate driving method of "two stop-and-go gate driving (2S&G)" to solve the problem.

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II. Measurement Setup and Definition of Different Gate Drive Methods

Figs. 1 and 2 show a circuit schematic and a photo of the measurement setup of the double pulse test for the automotive IGBT module at 300 V and 150 A, respectively. 6-bit DGD IC includes 63 parallel-connected pMOSFETs and 63 parallel-connected nMOSFETs. A 6-bit control signal n_{PMOS} [5:0] and n_{NMOS} [5:0] control how many of the 63 parallel-connected pMOSFETs and nMOSFETs are turned on, respectively. In this paper, the number of turned-on pMOSFETs and nMOSFETs are defined as n_{PMOS} and n_{NMOS}, respectively, where they are integers from 0 to 63. At turn-on, $n_{NMOS} = 0$ is fixed and n_{PMOS} is varied; the design value of $I_G = n_{PMOS} \times 79$ mA. At turn-off, $n_{PMOS} = 0$ is fixed and n_{NMOS} is varied; the design value of $I_G = n_{NMOS} \times 79$ mA.

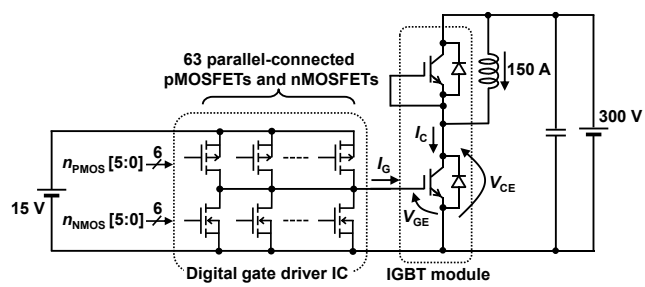

Fig. 1: Circuit schematic of double pulse test for automotive IGBT module.

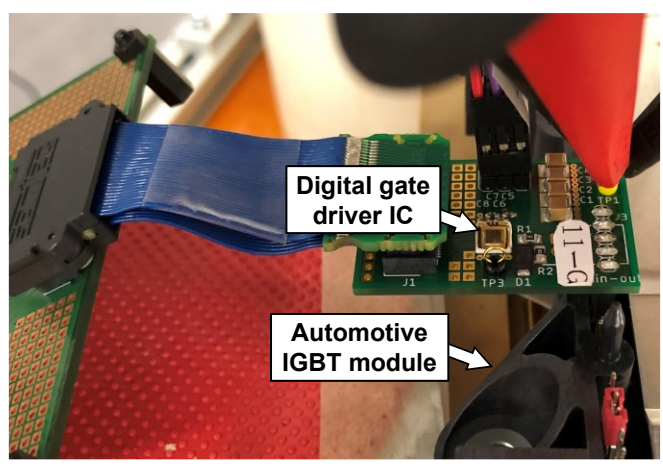

Fig. 2: Photo of measurement setup.

2022 IEEE 7th Southern Power Electronics Conference (SPEC) | 979-8-3503-9988-2/22/$31.00 ©2022 IEEE | DOI: 10.1109/SPEC55080.2022.10058383

A. Turn-on

At turn-on, five different gate driving methods shown in Fig. 3 are compared, and it will be shown that the proposed 2S&G shows the best performance. The 6-bit DGD IC is used to achieve five different gate driving methods shown in Fig. 3 with different time slot lengths and gate vectors (n_1 to n_{21} are integers from 0 to 63) during 400 ns at turn-on. Fig. 3 (a) shows the conventional single-step gate driving (CSG) with one parameter, which emulates the conventional fixed gate resistance gate driving method. Figs. 3 (b) and (d) show 1S&G with one parameter, where the uneven two slot lengths are determined by [1], and a 5 variable digital gate driving (5DG) with 100 ns × 4 slots and last long slot, respectively, which are proposed in [1]. Fig. 3 (e) shows a 21 variable digital gate driving (21DG) with 20 ns × 20 slots and last long slot as the ultimate digital gate driving. Fig. 3 (c) shows the proposed 2S&G with two parameters (n_1 and n_3), where the uneven four slot lengths are determined by analyzing the best gate vector of 21DG shown later in Table I . The name of 2S&G comes from the inclusion of two gate current zeros ($n_{PMOS} = 0$).

B. Turn-off

At turn-off, four different gate driving methods shown in Fig. 4 are compared, and it will be shown that the proposed 2S&G is not required. The 6-bit DGD IC is used to achieve four different gate driving methods shown in Fig. 4 with different time slot lengths and gate vectors (n_1 to n_{21} are integers from 0 to 63) during 800 ns at turn-off. Fig. 4 (a) shows CSG. Figs. 4 (b) and (c) show 1S&G [1], and 5DG with 200 ns × 4 slots and last long slot, respectively. Fig. 4 (d) shows 21DG with 40 ns × 20 slots and last long slot as the ultimate digital gate driving.

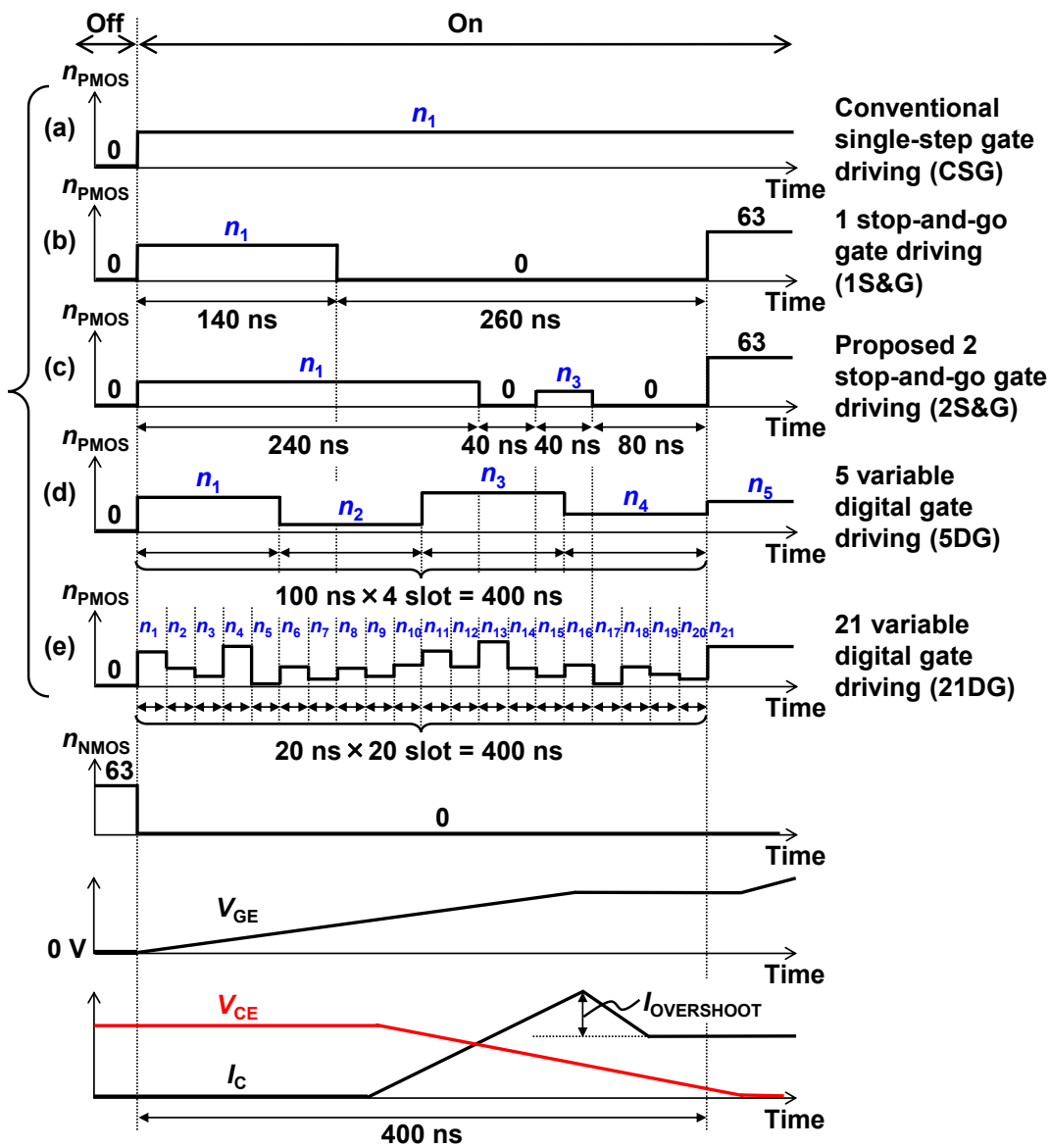

Fig. 3: Five different gate driving methods compared at turn-on. (a) Conventional single-step gate driving (CSG). (b) One stop-and-go gate driving (1S&G). (c) Proposed two stop-and-go gate driving (2S&G). (d) 5 variable digital gate driving (5DG). (e) 21 variable digital gate driving (21DG).

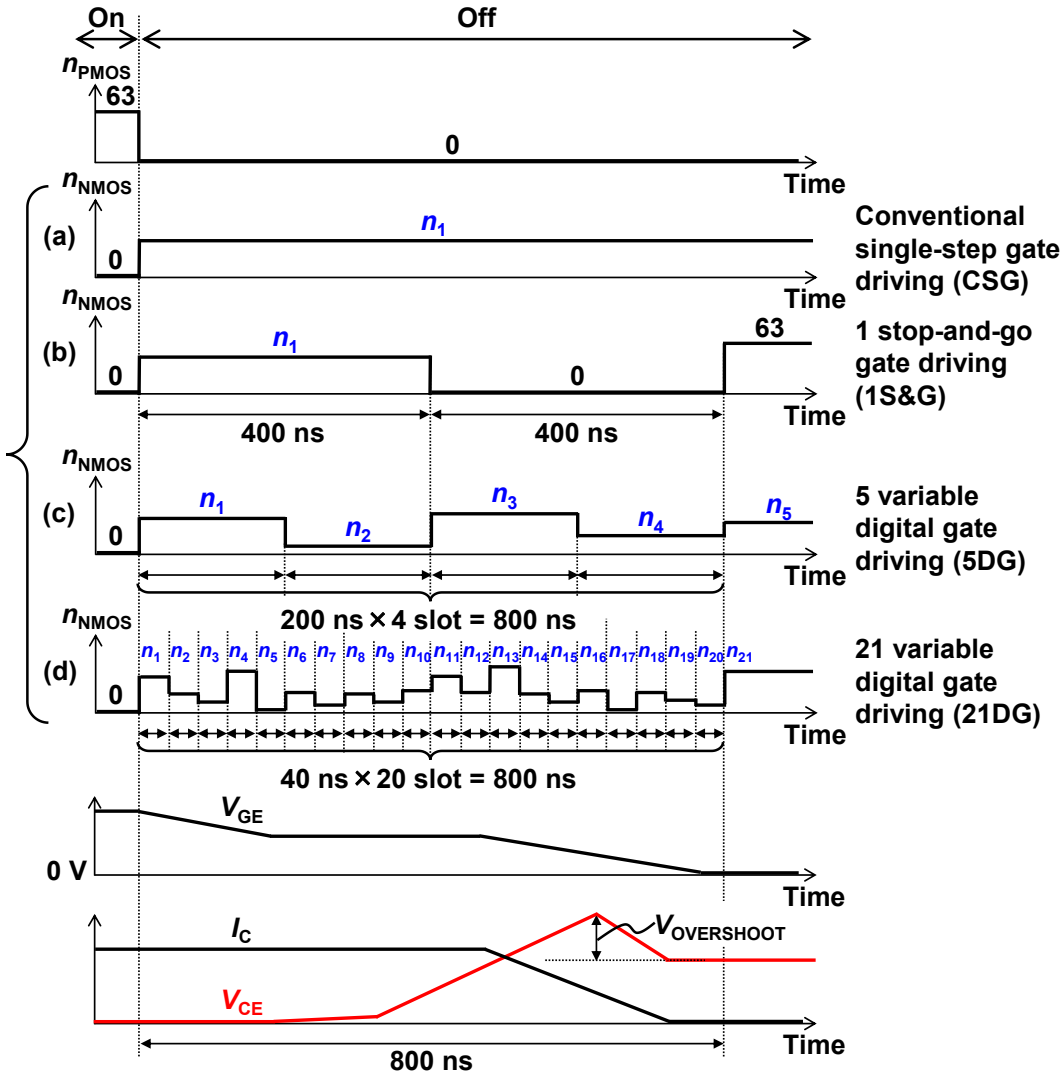

Fig. 4: Four different gate driving methods compared at turn-off. (a) Conventional single-step gate driving (CSG). (b) One stop-and-go gate driving (1S&G). (c) 5 variable digital gate driving (5DG). (d) 21 variable digital gate driving (21DG).

III. Measured Comparison of Different Gate Drive Methods

A. Turn-on

Fig. 5 shows the measured switching loss (E_{LOSS}) vs. collector current overshoot ($I_{OVERSHOOT}$) at turn-on. The five different gate driving methods are compared. In this paper, an evaluation function (f_{OBJ}) shown in Eq. (1) is defined as a performance index of gate driving, and it is discussed that a gate driving with small f_{OBJ} is an excellent gate driving with small E_{LOSS} and $I_{OVERSHOOT}$.

$$f_{OBJ} = \sqrt{\left(\frac{E_{LOSS}}{E_{LOSS,\,MAX}}\right)^2 + \left(\frac{I_{OVERSHOOT}}{I_{OVERSHOOT,\,MAX}}\right)^2} \qquad (1)$$

where the subscript MAX signifies the maximum of the corresponding quantity. The dotted concentric curves in Fig. 5 show the contour of $f_{OBJ.}$ Table I shows the details of Points A to F in Fig. 5 and the ranking of $f_{OBJ.}$ The black curve in Fig. 5 shows the trade-off curve of CSG with varied n_1 from 3 to 63. Points C and D are the best points that achieved the smallest f_{OBJ} with all search measurements of n_1, n_1 and n_3 in 1S&G and 2S&G, respectively. The analysis of $(2^6)^2$ measurements shows that n_1 optimization is important for 2S&G, while n_3 optimization is not. Therefore, the test cost of 2S&G is low because the optimization of n_3 can be omitted and only the optimization of n_1 is needed. Points E and F are the best points where the smallest f_{OBJ} is achieved by repeatedly measuring and searching for n_1 to n_5 and n_1 to n_{21} using the simulated annealing algorithm [2] for 5DG and 21DG, respectively. Specifically, 21DG took 14411 measurements (note that this is much smaller than the number of 64^{21} ($> 10^{37}$) combinations) over 12 hours and 30 minutes to complete the search. As shown in Table I, f_{OBJ} ranks the proposed 2S&G in first place, 21DG in second place, 5DG in third place, and 1S&G in fourth place, with the proposed 2S&G showing the best performance. Points A and B are CSG

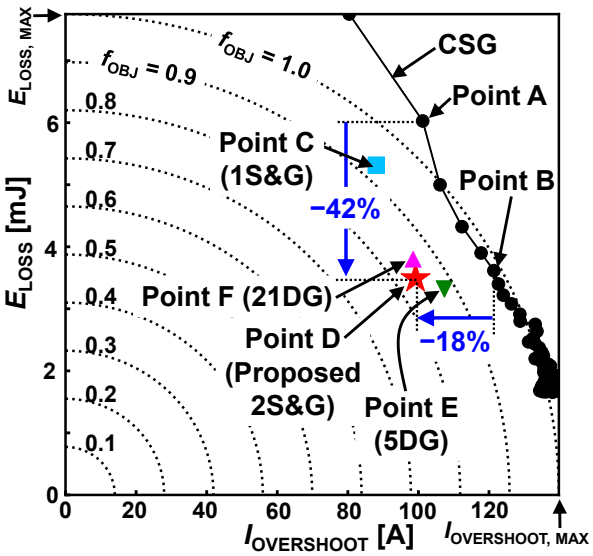

Fig. 5: Measured E_{LOSS} vs. $I_{OVERSHOOT}$ at turn-on. Five different gate driving methods are compared.

TABLE I. DETAILS OF POINTS A TO F IN FIG. 5 AT TURN-ON

	Gate driving method	Gate vectors	E_{LOSS} [mJ]	$I_{OVERSHOOT}$ [A]	f_{OBJ}	Ranking of f_{OBJ}
Point A	CSG	n_1 = 4	6.0	101	1.06	6th
Point B	CSG	n_1 = 8	3.6	121	0.99	5th
Point C	Best point in 1S&G	n_1 = 41	5.3	88	0.93	4th
Point D	Best point in proposed 2S&G	(n_1, n_3) = (20, 44)	3.5	99	0.83	1st
Point E	Best point in 5DG	(n_1, n_2, n_3, n_4, n_5) = (32, 39, 0, 35, 52)	3.3	107	0.88	3rd
Point F	Best point in 21DG		3.8	99	0.86	2nd

n_1	n_2	n_3	n_4	n_5	n_6	n_7	n_8	n_9	n_{10}	n_{11}	n_{12}	n_{13}	n_{14}	n_{15}	n_{16}	n_{17}	n_{18}	n_{19}	n_{20}	n_{21}
0	25	32	60	37	11	14	59	60	46	0	0	33	5	0	24	0	0	35	37	62

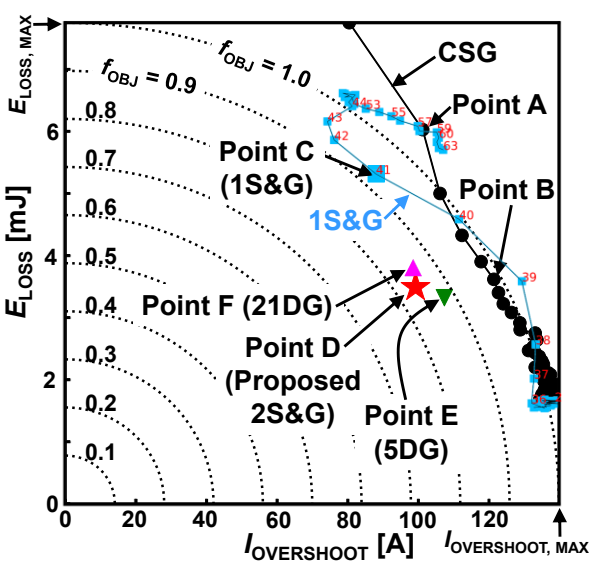

Fig. 6: Measured E_{LOSS} vs. $I_{OVERSHOOT}$ at turn-on. In 1S&G, n_1 is varied from 0 to 63. Red numbers indicate n_1.

points with $I_{OVERSHOOT}$ and E_{LOSS} approximately the same as the proposed Point D, respectively. As shown in Fig. 5, compared with CSG (Points A and B), the proposed 2S&G (Point D) reduces E_{LOSS} from 6.0 mJ to 3.5 mJ by 42 % under $I_{OVERSHOOT}$-aligned condition and reduces $I_{OVERSHOOT}$ from 121 A to 99 A by 18 % under E_{LOSS}-aligned condition.

To analyze 1S&G in detail, Fig. 6 shows measured E_{LOSS} vs. $I_{OVERSHOOT}$ of the five different gate driving methods. In 1S&G, n_1 is varied from 0 to 63. Red numbers in Fig. 6 indicate n_1. Since the trajectory of 1S&G is far from the proposed 2S&G (Point D), it is clear that 1S&G is inferior to 2S&G.

Fig. 7 shows the gate vectors and measured waveforms from Points A to F. Here the reasons why E_{LOSS} of 1S&G (Point C) is larger than that of the proposed 2S&G (Point D) are discussed. In 1S&G in Fig. 7 (c), the negative dI_C / dt during the 260-ns n_{PMOS} = 0 period causes V_{CE} overshoot, resulting in large E_{LOSS}, while the proposed 2S&G in Fig. 7 (d) successfully reduces E_{LOSS} by inserting a slot with n_{PMOS} = 44 during 160 ns to increase V_{GE} and decrease V_{CE} rapidly.

B. *Turn-off*

Fig. 8 shows the measured E_{LOSS} vs. collector-to-emitter voltage overshoot ($V_{OVERSHOOT}$) at turn-off. The four different gate driving methods are compared. In this paper, an evaluation function (f_{OBJ}) shown in Eq. (2) is defined as a performance index of gate driving, and it is discussed that a gate driving with small f_{OBJ} is an excellent gate driving with small E_{LOSS} and $V_{OVERSHOOT}$.

$$f_{OBJ} = \sqrt{\left(\frac{E_{LOSS}}{E_{LOSS,\,MAX}}\right)^2 + \left(\frac{V_{OVERSHOOT}}{V_{OVERSHOOT,\,MAX}}\right)^2} \tag{2}$$

where the subscript MAX signifies the maximum of the corresponding quantity. The dotted concentric curves in Fig. 8 show the contour of f_{OBJ}. Table II shows the details of Points G to K in Fig. 8 and the ranking of f_{OBJ}. The black curve in Fig. 8 shows the trade-off curve of CSG with varied n_1 from 3 to 63. Point I is the best points that achieved the smallest f_{OBJ} with all search measurements of n_1 in 1S&G. Points J and K are the best points where the smallest f_{OBJ} is achieved by repeatedly measuring and searching for n_1 to n_5 and n_1 to n_{21} using the simulated annealing algorithm [2] for 5DG and 21DG, respectively. Specifically, 21DG took 3098 measurements over 2 hours and 40 minutes to complete the search. As shown in Table II, f_{OBJ} ranks 5DG in first place, 21DG in second place, 1S&G in third place, which is a similar result to [1] in that f_{OBJ}'s of 5DG and 1S&G are almost the same. Points G and H are CSG points with $V_{OVERSHOOT}$ and E_{LOSS} approximately the same as Point J, respectively. As shown in Fig. 8, compared with CSG (Points G and H), 5DG (Point J) reduces E_{LOSS} from 21.2 mJ to 12.4 mJ by 42 % under $V_{OVERSHOOT}$-aligned condition and reduces $V_{OVERSHOOT}$ from 162 A to 85 A by 48 % under E_{LOSS}-aligned condition.

To analyze 1S&G in detail, Fig. 9 shows measured E_{LOSS} vs. $V_{OVERSHOOT}$ of the four different gate driving methods. In 1S&G, n_1 is varied from 0 to 63. Red numbers in Fig. 9 indicate n_1. Since the trajectory of 1S&G passes close to 5DG (Point J), the

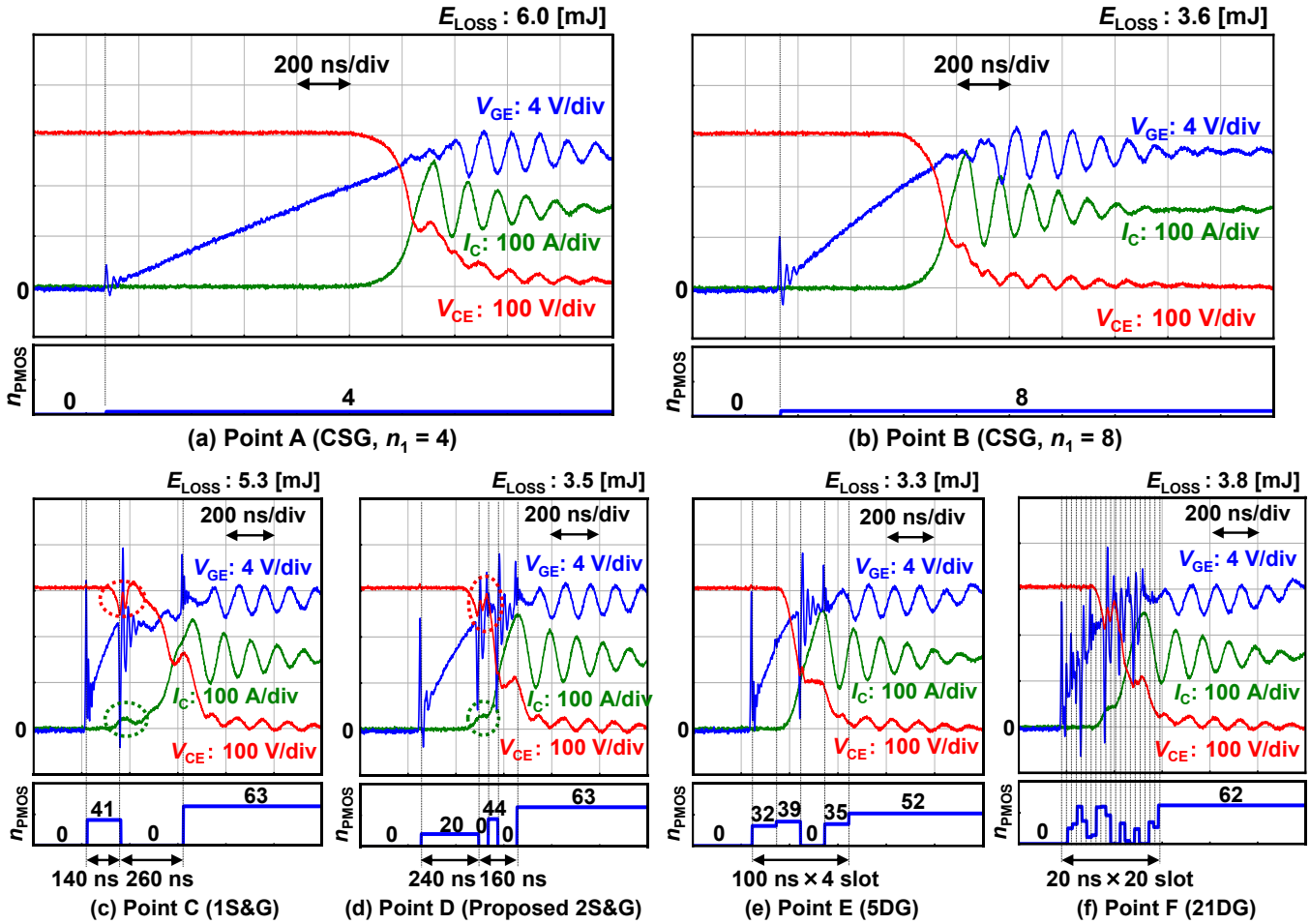

Fig. 7: Gate vectors and measured waveforms from Points A to F at turn-on.

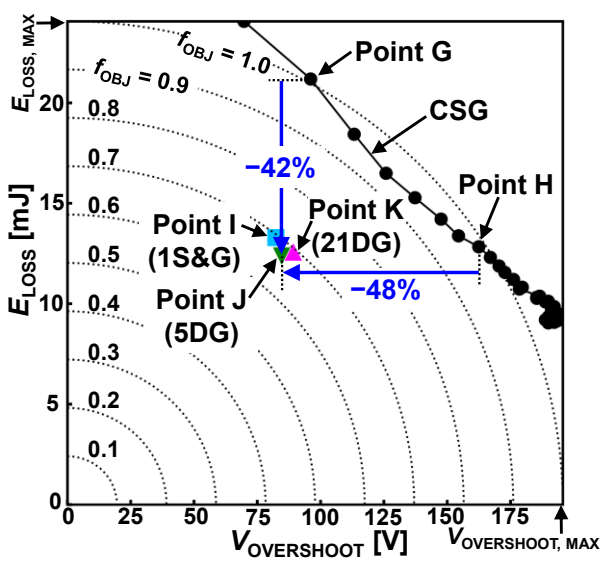

Fig. 8: Measured E_{LOSS} vs. $V_{OVERSHOOT}$ at turn-off. Four different gate driving methods are compared

TABLE II. DETAILS OF POINTS G TO K IN FIG. 8 AT TURN-OFF

	Gate driving method	Gate vectors	E_{LOSS} [mJ]	$V_{OVERSHOOT}$ [V]	f_{OBJ}	Ranking of f_{OBJ}
Point G	CSG	n_1 = 4	21.2	96	1.03	5th
Point H	CSG	n_1 = 10	12.3	162	0.97	4th
Point I	Best point in 1S&G	n_1 = 45	13.3	82	0.70	3rd
Point J	Best point in 5DG	(n_1, n_2, n_3, n_4, n_5) = (63, 33, 0, 3, 18)	12.4	85	0.67	1st
Point K	Best point in 21DG		12.6	89	0.69	2nd

n_1	n_2	n_3	n_4	n_5	n_6	n_7	n_8	n_9	n_{10}	n_{11}	n_{12}	n_{13}	n_{14}	n_{15}	n_{16}	n_{17}	n_{18}	n_{19}	n_{20}	n_{21}
33	53	20	32	36	9	60	41	25	63	26	45	1	0	0	0	0	48	5	0	6

performance of 1S&G and 5DG is almost identical and 1S&G is more practical than 5DG because of the lower test cost, which is the same conclusion as [1].

Fig. 10 shows the gate vectors and measured waveforms from Points G to K. A common trend among Points I to K is to set n_{NMOS} to zero just before $V_{OVERSHOOT}$ occurs, thereby successfully achieving both low E_{LOSS} and low $V_{OVERSHOOT}$, which is the same conclusion as [1]. Here the reasons why the proposed 2S&G is required for turn-on, but not for turn-off, are discussed. At turn-on of 1S&G shown in Fig. 7 (c), during the 260-ns n_{PMOS} = 0 period, I_C does not increase monotonically, but

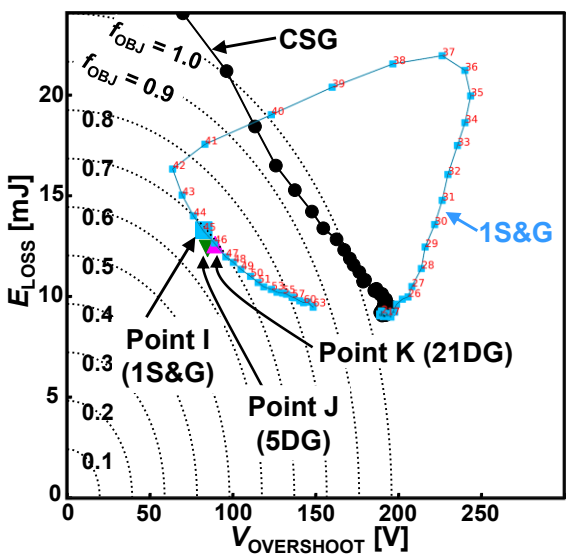

Fig. 9: Measured E_{LOSS} vs. $V_{OVERSHOOT}$ at turn-off. In 1S&G, n_1 is varied from 0 to 63. Red numbers indicate n_1.

drops once in the middle. In contrast, at turn-off of 1S&G shown in Fig. 10 (c), during the 400-ns n_{NMOS} = 0 period, I_C decreases monotonically. Thus, it is concluded that the proposed 2S&G is required for turn-on, where I_C change is not monotonic, while the proposed 2S&G is not required for turn-off, where I_C change is monotonic.

IV. Conclusions

This paper shows that the conventional 1S&G does not work effectively in the turn-on of the large-capacity automotive IGBT (1200 V, > 200 A rating), and proposes a new active gate driving method of 2S&G to solve the problem. It is concluded that the proposed 2S&G is required for turn-on, where I_C change is not monotonic, while the proposed 2S&G is not required for turn-off, where I_C change is monotonic. In the turn-on measurements, compared with CSG, the proposed 2S&G with low test cost reduces E_{LOSS} by 42 % under $I_{OVERSHOOT}$-aligned condition and reduces $I_{OVERSHOOT}$ by 18 % under E_{LOSS}-aligned condition at 300 V and 150 A.

Acknowledgment

This work was partly supported by New-generation Power Electronics and System Research Consortium Japan (NPERC-J), FS research (PJ-08).

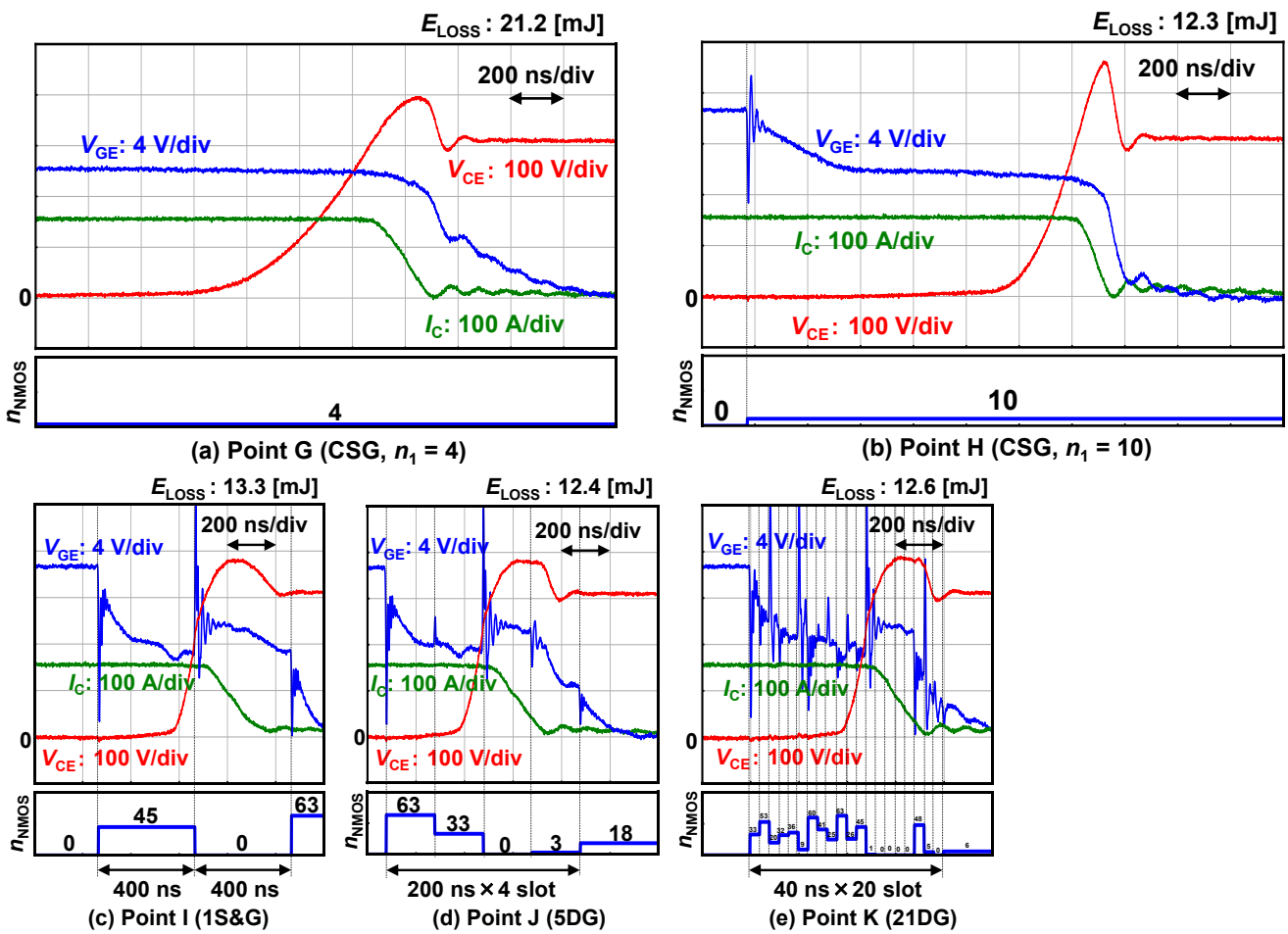

Fig. 10: Gate vectors and measured waveforms from Points G to K at turn-off.

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